AMENDMENTS TO THE CLAIMS

1. (previously presented) A non-volatile memory device comprising:

an array of non-volatile memory cells, wherein the array comprises bit lines coupled to the non-volatile memory cells;

sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines, wherein the bit lines are pre-charged to different voltage levels prior to accessing a memory cell;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections; and

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal.

2. (original) The memory device of claim 1 and further comprising input circuitry to receive input data on the data connection on rising and falling edges of the clock signal.

3. (original) The memory device of claim 1 wherein the array of non-volatile memory cells is arranged in a plurality of addressable banks.

4. (original) The memory device of claim 3 wherein each addressable bank contains addressable sectors of memory cells.

5. (original) The memory device of claim 1 wherein the memory is adapted to provide burst-oriented read accesses.

6. (original) The memory device of claim 1 wherein the output circuitry is further adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

7. (canceled)

8. (previously submitted) A flash memory device comprising:

an array of non-volatile memory cells, wherein the array comprises bit lines coupled to the non-volatile memory cells;

sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell, wherein the pre-charge circuitry pre-charges an active digit line that is coupled to a read memory cell to a voltage that is greater than a complementary digit line;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented; and

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal, the output circuitry is further adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

9. (canceled)

10. (original) The flash memory of claim 8 wherein the pre-charge circuitry pre-charges the digit lines to a differential level using charge sharing.

11. (original) The flash memory of claim 8 wherein the pre-charge circuitry pre-charges the digit lines to a differential level using a bias circuit.

12. (currently amended) A processing system comprising:

a processor; and

a rambus dynamic random access memory (RDRAM) compatible non-volatile memory device coupled to the processor comprising:

an array of non-volatile memory cells, wherein the array comprises bit lines coupled to

the non-volatile memory cells;

sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell;

a clock signal connection to receive a clock signal;

an RDRAM interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented; and

output circuitry to provide output data on the data connections on rising ~~risign~~ and falling edges of the clock signal, the output circuitry is further adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

13. (original) The system of claim 12 wherein the processor generates flash memory compatible control signals.

14. (canceled)

15. (original) The system of claim 12 wherein the processor is adapted to receive burst transmissions of data from the memory device.

16. (original) The system of claim 12 wherein the non-volatile memory device is a flash memory device.

17. (original) The system of claim 12 wherein the memory cells are floating gate memory cells.

18. (original) The system of claim 12 wherein the processor generates computer system commands.

19. (original) The system of claim 12 wherein the pre-charge circuitry pre-charges the digit lines to a differential level using either charge sharing or a bias circuit.

20. (original) The system of claim 12 and further including a unified communication bus coupling the processor with the RDRAM compatible non-volatile memory device and volatile memory devices.